MPC5200 Microprocessor Technical Summary

The MPC5200 is a highly integrated, cost-effective, 760 MIPS embedded PowerPC® processor that operates at just one watt at 400 MHz. It offers integrated Ethernet, USB, CAN, Serial, I^2C, I^2S, SPI, AC97 CODEC interface, J1850, ATA, and PCI. System throughput is enhanced by a BestComm™ intelligent DMA unit that significantly off loads the processor core from routine I/O tasks. The 400 MHz MPC603e core processes 760 Dhrystone 2.1 MIPS and is further augmented by an on-chip double-precision Floating Point Unit (FPU). An integrated Double Data Rate (DDR) memory controller further boosts data movement. This combination of I/O, processing power, and data throughput enhancements makes the MPC5200 well suited for telematics, gateways, industrial control, Internet-access devices, video detection and processing, and electronic/medical instrumentation.

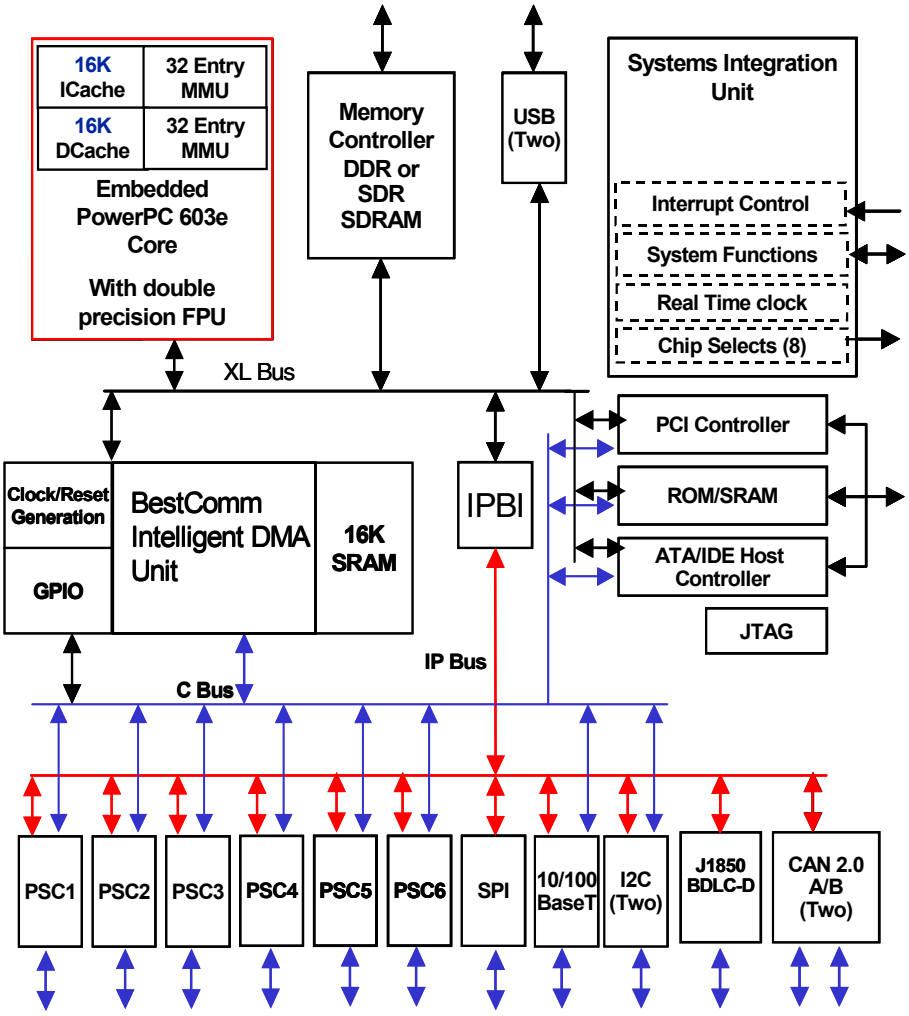

Figure 1. MPC5200 Block Diagram

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With the success of the MPC5200 in the automotive market, other markets can now enjoy extended automotive temperature qualification and life cycles typically found in that industry. The MPC5200 is engineered to support an external dual-bus architecture with a separate high-speed SDRAM/DDR controller used primarily by the PowerPC processor core. A Peripheral Component Interconnect (PCI) compatible interface may be used as a generalized interface to system level peripherals in addition to the ATA/IDE interface which provides access to disk drives.

1 Key Features

MPC603e series PowerPC core

- Superscalar architecture
- 0 – 400 MHz static operation MPC5200CBV400
  (-40°C to +85°C temperature range)
- 0 – 400 MHz static operation MPC5200BV400
  (0°C to +70°C temperature range)
- 16 K Instruction / 16 K Data Caches
- Double-precision FPU
- Instruction and Data MMU
- Dynamic power management including Doze and Sleep modes
- 159 microseconds to first instruction execution at power-on at 400 MHz
- Standard & critical interrupt capability

High speed SDRAM memory interface

- 133 MHz operation (266 MHz effective with DDR)
- SDR & DDR SDRAM support
- 256 Mbyte addressing range
- 32-bit data bus
- Built-in initialization and refresh

Flexible multi-function external bus

- Supports PCI, ATA/IDE, and ROM/RAM/Flash interfaces
- Version 2.2 PCI master compatibility
  - 32-bit multiplexed address/data
  - 66 MHz operation with BestComm enabled
- Version 4 ATA compatible external interface
- IDE Disk Drive connectivity
- ROM/RAM/Flash interface
  - Boot ROM, external peripheral connectivity
  - Non multiplexed data access using 8/16/32 bit databus with up to 26 bit address bus

- Multiplexed data access using up to 32 bit data with 25 bit addresses + 2 Bank bits

BestComm I/O subsystem

- BestComm virtual DMA controller
- Dedicated DMA channels for reception and transmission for nearly all peripheral interfaces
- Programmable Serial Controllers (PSCs)
  - UART or Serial Interface
  - CODEC interface for modem, generic CODEC or AC97 audio
  - Suitable for Bluetooth® modules, cellular, GPS, digital radio interface, etc.
  - Configurable as I^2S ports
- 10/100 BaseT Ethernet
- USB Master 1.1 with OHCI support
  - Support for two independent master USB ports
- I^2C Controller(s) to 520 Kbps
  - Support for two independent I^2C ports
- Serial Peripheral Interface (SPI) controller

Dual MSCAN 2.0 A/B Controller modules

- Freescale Scalable Controller Area Network (MSCAN) architecture
- V2.0 A/B CAN protocol
- Standard and extended data frames
- Programmable bit rate up to 1Mbps

Byte Data Link Controller - Digital BDLC-D

- J1850 Class B data communication network interface compatible and ISO compatible for low speed (<125 Kbps) serial data communications in automotive applications.
- 10.4 Kbps variable pulse width (VPW) bit format
- Digital noise filter
- Collision detection
- Hardware Cyclical Redundancy Check (CRC) generation and checking
- Two power saving modes with automatic wakeup on network activity
- Polling and CPU interrupt available
- Block mode receive/transmit supported
- Supports 4X mode, 41.6 Kbps
- In-frame Response (IFR) types 0, 1, 2, and 3 supported
- Wakeup on J1850 message

System level features

- Up to eight programmable chip selects

- Interrupt controller
  - Four external interrupt request lines supporting standard and/or critical interrupts
  - Support for all other internal interrupt sources
- GPIO / Timer functions
  - Two GPIO pins supporting wakeup capability
  - Up to eight GPIO pins with timer capability supporting Input Capture, Output Compare, and Pulse Width Modulation (PWM) functions
  - Up to 56 total GPIO pins (depending on functional multiplexing selections)
- Systems Protection (watch dog timer, bus monitor)
- Real-time clock
- Power management features

Test / Debug features

- JTAG (IEEE 1149.1 test access port)
- Common On-Chip Processor (COP) debug port

On-board PLL and clock generation

Software Development Support

- Complete software development tool chain
- Optional accessory development kits
- Robust silicon evaluation kits
- Technical support
- Professional services

2 Physical Characteristics

- 1.5V internal, 3.3V external operation (2.5V for DDR interface)
- TTL compatible I/O pins
- Full performance extended Temperature Range (-40 to +85 C)
- Commercial Temperature Range MPC5200BV400 (0 C to +70 C)
- 272-pin plastic ball grid array (PBGA), 1.27 mm ball pitch

3 Architecture Overview

The MPC5200 is optimal for price sensitive, low-power embedded application requiring a single chip solution. Due to its success in the automotive market, it also helps to ensure long-term availability. Building on Freescale Semiconductor, Inc. (formerly Freescale) success in the automotive market with the MPC5200, the device optimizes the processing power and peripheral mix for both mobile and fixed applications in markets for telematics, gateways, industrial control, video detection and processing, and

electronic/medical instrumentation. The part has been qualified for extended temperature use for the telematics and industrial control markets.

The MPC5200 integrates an enhanced high-performance MPC603e series PowerPC processor core with double-precision FPU with an I/O subsystem containing the BestComm intelligent DMA unit. BestComm is capable of responding to peripheral interrupts independent of the processing core and provides low-level peripheral management, protocol processing and peripheral data movement functions.

The MPC5200 has a high speed DDR SDRAM controller designed to support an external memory interface dedicated to the processor, allowing optimized instruction and data bursting. The dedicated memory interface, coupled with on-chip 16 Kbyte instruction and 16 Kbyte data caches designed to enable cache-sensitive software environments, such as Java®, to run in real time while leaving plenty of processing power for peripheral management and system control tasks.

The MPC5200 also contains a PCI compatible external bus. This bus allows connection to a wide variety of external peripheral devices including graphics controllers or CMOS camera devices. There is also an ATA/IDE interface for support of external drives. Additionally, there is a ROM/Flash interface for support of boot file and program/data storage.

The MPC5200 has an optimized peripheral mix to support today's more full-featured products. There are six programmable serial channels (four configurable as I^2S), one SPI, one 10/100 BaseT Ethernet, and a programmable number of general-purpose I/O channels (GPIOs) supported directly by the BestComm I/O subsystem. The low-level data movement and protocol processing tasks for these peripheral functions are handled independently of the PowerPC processor core by the BestComm module. BestComm has a dedicated DMA channel for each of these peripheral interfaces allowing incoming and outgoing data to be organized efficiently in external memory for use by the PowerPC processor core.

In addition, there are two USB, two I^2C, one BDLC-D (J1850), and two MSCAN 2.0B channels available on the internal processor bus. Together, this array of diverse integrated I/O allow for very cost effective system solutions for highly networked products and applications.

A sophisticated external multiplexing scheme allows the highly integrated design to fit in a low-cost 272-pin PBGA package, dramatically lowering overall device footprint and system costs.

4 Embedded PowerPC Processor Core

The MPC5200 core is derived from Freescale's (fromerly Freescale) MPC603e family of Reduced Instruction Set Computer (RISC) microprocessors. The core is a high-performance, low-power implementation of this superscalar architecture. It contains 16 Kbytes of instruction cache and 16 Kbytes of data cache. Caches are four-way associative and use the Least Recently Used (LRU) replacement algorithm.

The core contains four independent execution units: Branch Processing Unit (BPU), Integer Unit (IU), Load and Store Unit (LSU), and System Register Unit (SRU). Up to three instructions can be issued and tiered per clock. Most instructions execute in a single cycle. It contains an integrated, double-precision FPU, which is well suited to processing video, audio, or data files. It has two Memory Management Units (MMUs), one for each cache. The core implements the 32-bit portion of the superscalar architecture which provides 32-bit effective addresses and integer data types of 8, 16, and 32 bits.

Enhancements to the standard MPC603e core include:

- Exceptional interrupt latency (critical interrupts)
- 8 Advanced MMU BAT (16 total) registers and 1 Kbyte page management

5 BestComm DMA I/O Subsystem

BestComm contains an intelligent DMA unit, which provides a front-line interrupt control and data movement interface via a separate peripheral bus to the on-chip peripheral functions. This leaves the PowerPC processor core free to handle higher level activities. The concurrent operation offers a significant boost in overall system performance.

BestComm is designed to support up to 16 simultaneously enabled DMA tasks from up to 32 DMA requestors. BestComm uses internal buffers to prefetch “reads” and post “writes” such that bursting is used whenever possible. This optimizes both internal and external bus activities.

6 Programmable Serial Controllers (PSC)

Six full-duplex channels are engineered to support both asynchronous and synchronous protocols for both 8-bit and 16-bit data formats. They may be used to connect to a wide variety of devices, including RS232 and UART-based peripherals, CODECs (master and slave modes), Bluetooth® modules, cellular modules, navigation/GPS, 2-way pagers, or a standard UART interface to a terminal/computer for debug support. Four of the PSCs may be configured to support I^2S in master or slave modes.

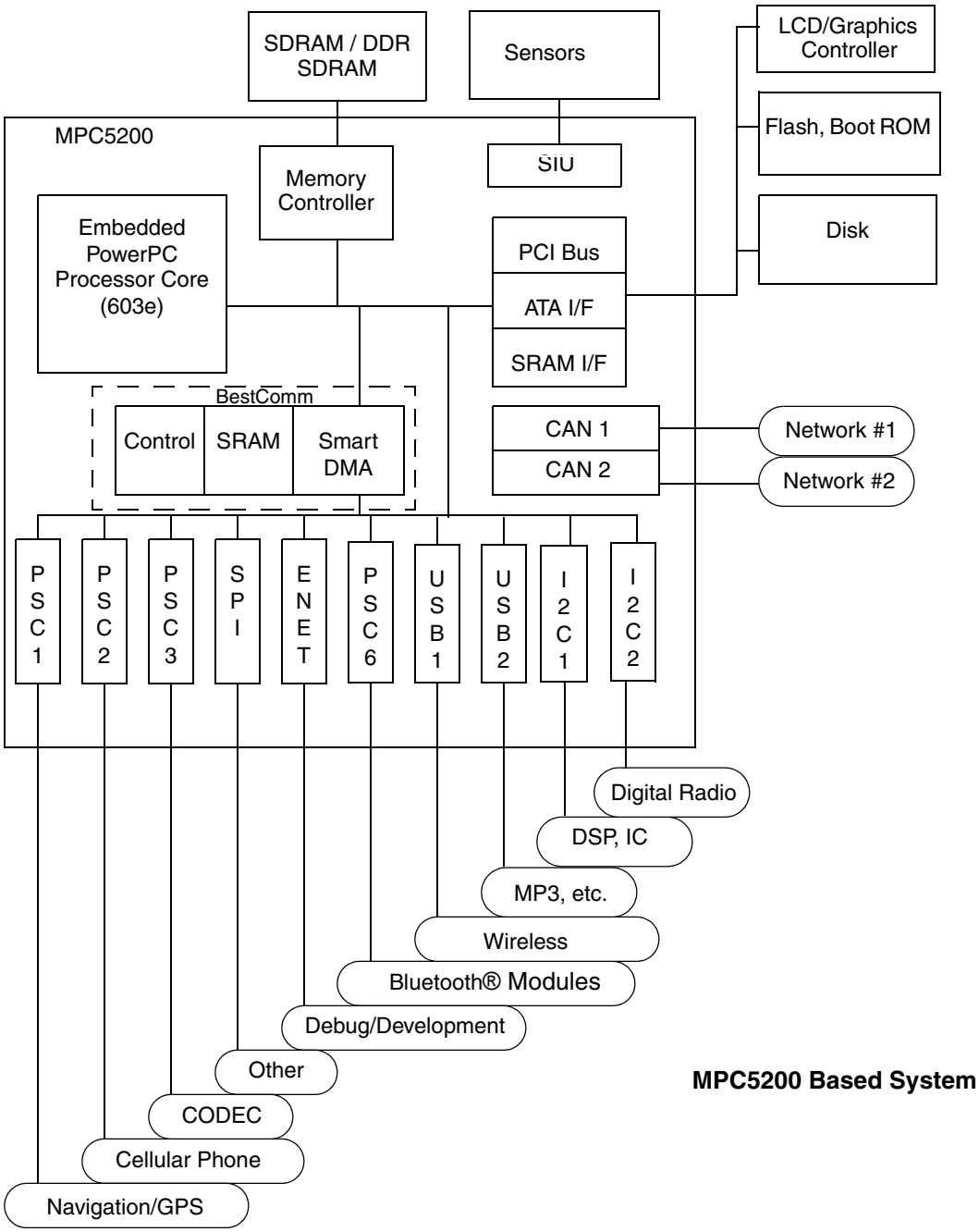

Figure 2. Example MPC5200 Based System Block Diagram

7 10/100 BaseT Ethernet

Designed to support standard MAC-PHY interfaces: 10 Mbps and 100 Mbps IEEE 802.3 MII and 10 Mbps 7-wire interface for debug and communication.

8 ^{2}C (Inter Integrated Circuit)

Contains two separate multi-master, microwire compatible I^2C interfaces and is designed to support 520 Kbps transfer rates. Both master and slave interfaces may be controlled directly by the PowerPC processor core or can utilize the BestComm subsystem to buffer tx/rx data when the I^2C interrupt frequency is high.

9 SPI (Serial Peripheral Bus)

Full duplex, synchronous serial communication interface. It is designed to support master and slave modes, double-buffered operations, and to operate in polling and interrupt driven environments.

10 USB (Universal Serial Bus)

Implements the USB Host Controller/Root Hub in compliance with the USB 1.1 specification. Supports one or two USB ports off of the root hub which then connects to an off-chip USB transceiver. The host controller supports the Open Host Controller Interface (OHCI) standard.

11 System Level Interfaces

The MPC5200 integrates the most common system interfaces and signals. There are up to eight fully programmable external chip selects, independent of the SDRAM interface. CS0 has special features to help support a Boot ROM. The interrupt controller is provided with four external interrupt signals. The controller manages external and internal interrupts. Levels and priorities of all interrupts are programmable. The interrupt controller is designed to take advantage of the advanced PowerPC processor core critical interrupt feature. This allows interrupting of the PowerPC processor core outside the operating system boundaries for critical real-time functions.

Several timer functions required by most embedded systems are integrated. Two internal Slice Timers are offered to create short cycle periodic interrupts. A Watch-Dog Timer is included which is designed to interrupt the processor if not regularly serviced, catching software hang-ups. A bus monitor is included to monitor bus cycles and to offer an interrupt if transactions take longer than a prescribed time.

There are ten dedicated GPIO signals, two of which are designed to support wakeup capability to the MPC5200 bringing it out of low power modes, eight of which can be attached to eight internal full function timers. Additionally, nearly all the pins of the MPC5200 may be configured as GPIO ports, so more are available depending on what MPC5200 I/O resources are utilized in a given design.

Many of the serial/parallel port pins serve multiple functions, allowing flexibility in optimizing the system to meet a specific set of integration requirements. For example, PSC3 could be dedicated to a 9-pin modem interface or could be split into a simple UART with five available GPIO pins.

12 Dual MSCAN (Freescale Scalable Controller Area Network)

The CAN is an asynchronous communications protocol used mostly in automotive and industrial control systems and other systems requiring high reliability and noise immunity. It is a high speed (1 Mbps), short distance, priority based protocol designed to run over a variety of media. The MSCAN is designed to support both the standard and extended identifier (ID) message formats. Each MSCAN module contains four receive buffers with FIFO storage scheme and three transmit buffers. It also contains flexible maskable identifier filters.

13 BDLC - D (Byte Data Link Controller - Digital J1850)

The BDLC controller is a serial communication module designed to allow the user to send and receive messages across a Society of Automotive Engineers (SAE) J1850 serial communication network. The user's software handles each transmitted or received message on a byte-by-byte basis, while the BDLC performs the network access, arbitration, message framing and error detection duties.

14 SDRAM Controller and Interface

A high speed SDRAM controller is engineered to support both standard SDRAM and Double Data Rate (DDR) SDRAM devices. It is engineered to support 64 Mbit, 128 Mbit, 256 Mbit, and 512 Mbit memories. Bursting is supported, allowing data transfer rates of 528 Mbytes/sec with SDR @ 133 MHz and 1056 Mbytes/sec with DDR memories at 133 MHz (266 MHz effective SDR rate)

15 Multi-function External Bus

The MPC5200 is engineered to support a multi-function external local bus to allow connections to PCI and ATA/IDE compliant devices as well as external ROM/SRAM. It integrates a 3.3V, PCI V2.2 compatible external bus controller and interface. This bus is a 32-bit multiplexed address/data bus designed to support PCI bus frequencies up to 66 MHz.

The external bus is also designed to support for an ATA/IDE disk drive interface. ATA control signals (chip selects, write, read, etc.) are provided which are independent of the PCI control signals to help prevent bus contention. The 32-bit data bus is shared. When it recognizes an external access meant for the ATA controller, the function of the PCI address/data bus is transformed into 16 bits of ATA data and 3 bits of ATA address.

The external bus is also designed to allow connection to external memory or peripheral devices that adhere to a ROM or SRAM-like interface. These devices occupy a separate location in the memory map and have separate control signals (chip select, transfer start, read/write, address latch enable and transfer acknowledge). When an internal access is decoded to fall within the memory mapped range of these devices, the local bus is engineered to be transformed to supply the appropriate address, data and control signals. Several different interface options are available and programmable on a per-chip basic. Some

options present address and data on the bus simultaneously (non-multiplexed modes). Other options present address first then data, in separate tenures (multiplexed mode). Multiplexed-mode options require external logic to latch the address. The following options are available:

Non-multiplexed Modes

- 16 bit Address, 16 bit Data (with PCI and ATA support)
- 24 bit Address, 8 bit Data (with PCI and ATA support)
- 26 bit Address, 8/16 bit Data - Large Flash Mode (no PCI support)
- 24 bit Address, 32 bit Data (no PCI or ATA support)

Multiplexed Modes

- 25 bit Address, 8/16/32 bit Data (with PCI and ATA support)

Bursting, dynamic bus sizing and BestComm DMA support are provided for the SRAM/ROM interface.

The MPC5200 is designed to support a reset configuration mode common on the family of microprocessors that implement the PowerPC architecture where 16 bits of configuration information is driven and sampled during reset to establish the initial processor configuration.

16 Power Management

The MPC5200 is manufactured in a low-power static CMOS technology. In addition, it is designed to support the dynamic power management modes available on the 603e series processors including doze and sleep modes.

Several of the GPIOs and interrupt lines are designed to support a wakeup capability such that the MPC5200 can be placed in a low power stand-by mode, then re-enabled by one of the wakeup inputs.

17 Systems Debug and Test

The MPC5200 is designed to support the COP debug capability common on other Freescale (fromerly Freescale) processors. The COP interface supports such features as memory download, single step instruction execution, break/watch point capability, access to internal registers, pipeline tracking, etc.

Supports a JTAG IEEE 1149.1 controller and Test Access Port (TAP).

18 Power Consumption

Typical Power Consumption at 400 MHz utilizing two concurrent tasks, memory copies and BestComm: Approximately one watt.

19 Time to First Instruction Execution from Power-on

159 microseconds at 400 MHz to execute the first instruction upon applying power to the MPC5200

20 More Information

Access for additional MPC5200 Information:

http://www.freescale.com or http://www.mobilegt.com/

Additional documentation:

Lite5200™ EVB Product Brief: MPC5200LITEPB/D

Lite5200 EVB Kit Product Brief: CWMPCEVB5200PB

mobile*GT* Total5200™ SDP Product Brief: MOBILEGT5200PB/D

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